IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Shreesh Narasimha, et al.

Examiner: Quang D. Vu

Serial No.: 10/763,308

Art Unit: 2811

Filed: January 23, 2004

Docket: FIS920020200US2 (16106A)

For: CMOS DEVICE INTEGRATION FOR LOW EXTERNAL RESISTANCE

Dated: September 27, 2004

Confirmation No.: 6529

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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RESPONSE UNDER 37 C.F.R. §1.111

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In response to the Office Action dated June 25, 2004, applicants submit the following amendments and remarks for entry of record in the above-identified patent application.

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CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8) Applicant(s): **Shreesh Narasimha, et al.**	Docket No. **FIS920020200US2 (16106A)**

Application No.	Filing Date	Examiner	Group Art Unit
10/763,308	**January 23, 2004**	**Quang D. Vu**	**2811**

Invention: **CMOS DEVICE INTEGRATION FOR LOW EXTERNAL RESISTANCE**

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Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/763,308	January 23, 2004	Quang D. Vu	23389	2811	6529

Invention: **CMOS DEVICE INTEGRATION FOR LOW EXTERNAL RESISTANCE**

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AMENDMENT TRANSMITTAL LETTER (Large Entity) Applicant(s): Shreesh Narasimha, et al.	Docket No. FIS920020200US2 (16106A)

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/763,308	January 23, 2004	Quang D. Vu	23389	2811	6529

Invention: **CMOS DEVICE INTEGRATION FOR LOW EXTERNAL RESISTANCE**

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